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Steps towards the realization of novel prototype functional devices using scanning probe microscopy

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1 Introduction

Moore's principle predicts that beyond the year 2010, the typical structure dimensions of electronic memory devices will fall below 70 nm. Apart from the necessity to develop suitable lithographic techniques for mass production of sub–100–nm features, the sole reduction of the structure dimensions (top–down approach), while maintaining the present–day device architecture, will result in physical obstacles, making the invention of novel designs for future devices indispensable. It what follows, we report on novel concepts for the fabrication of a single-electron transistor (SET) and a quantum–interference transistor (QUIT), respectively.

2 Novel concepts for functional devices

2.1 Single-electron transistor

An approach will be to use metallic nanoparticles with sizes below 30 nm as individual building blocks for the synthesis of novel functional devices by the controlled arrangement of the nanoparticles in a step–by–step fashion (bottom–up strategy). Deposited on suitable substrates, nanoparticles can be imaged, characterized, and manipulated using scanning probe microscopes (SPM) [1]. Fig. 1 shows an example for the atomic force microscope (AFM) assisted synthesis of a chain-like structure (Fig. 1b) of 20–nm–sized colloidal Au particles previously randomly deposited on a natively oxidized Si substrate (Fig. 1a); both images cover a range of 560 nm × 560 nm. Nanoparticles of less than 10 nm in diameter have successfully been used in studying single–electron phenomena, revealing pronounced steps in the scanning tunneling microscope (STM) recorded I–V characteristics at room temperature[2]. Moreover, by analyzing I–V curves taken on a pair arrangement of Ag nanoparticles deposited on a Si(111):H surface, an interaction of the two neighboring particles has been observed, most likely as a result of a mutual capacitive and/or resistive coupling[3].

Based on these experimental findings, nanoparticles are employed as individual building blocks to design devices having outstanding electrical properties which in turn can be tailored according to specific desires. Doing this, first the nanoparticles are randomly deposited on Si substrates covered with a several 100–nm–thick SiO_2 layer. On top of the SiO_2, electrodes are patterned by electron–beam lithography, followed by a metallization process and lift–off techniques. As a particularity, these electrodes are electrically interrupted by a gap of only a few 10 nm in width, thus forming source and

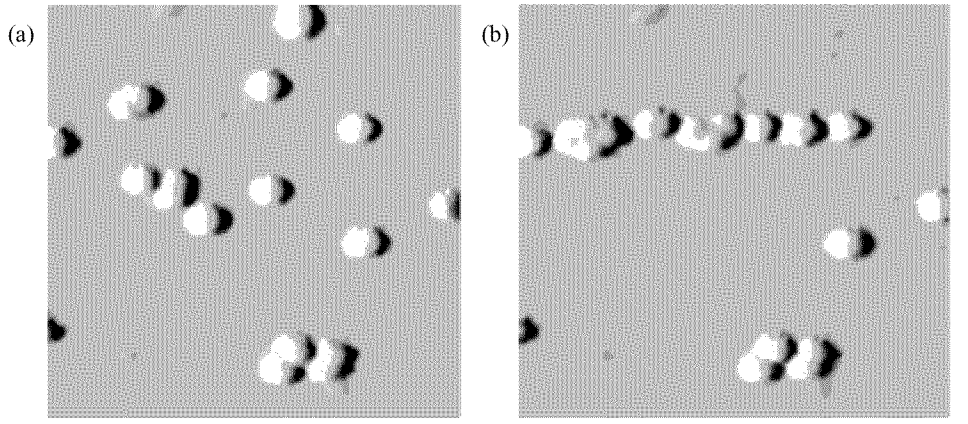

Fig 1. 20-nm-sized Au particles on a SiO_2 substrate, (a) initially randomly distributed and (b) after alining them with an AFM.

drain contacts. With the AFM, suitable nanoparticles can be selected and controllably be arranged within this gap region, so that the nanoparticles may electrically bridge source and drain. By using a three–electrode configuration (source, drain, and gate), where the gate couples capacitively to the particle arrangement, the pathway for electrons can be opened and closed, respectively, depending on the voltage applied to the gate electrode. More importantly, the electrical properties of this device can subsequently be modified by easily rearranging preselected nanoparticles with respect to their neighbors. The synthesized configuration represents a tunable prototype SET.

Referring to specialized applications, metallic lines in the 10–nm–range can directly be deposited in any desired pattern by locally decomposing an organometallic precursor in the electron beam provided by the tip of a STM operated in an ultra-high vacuum environment [4]. Following the decomposition of the precursor molecules, the metallic component is predominantly deposited onto the substrate surface and the remaining organic fragments are pumped off. While scanning the tip over the sample, 20–nm–wide conducting lines can be fabricated with lengths in the mm range (Fig. 2).

2.2 Quantum-interference transistor (QUIT)

Arranging the nanoparticles within the gap region of the three–electrode system in a ring structure results in the formation of the classical Aharonov–Bohm configuration. The resultant diameter of the assembled circle actually depends on the size of the nanoparticles used, but can be as small as a few 10 nm — overall dimensions which are not available with conventional lithographic techniques. Contacting this ring structure to source and drain properly allows electrons to wend their way along two possible pathways. If the total length of both pathways is shorter than the mean-free path or coherence length in the respect material, the wave nature of moving electrons are expected to give rise to interference phenomena. In particular, the electron wave properties might be affected in one branch, e.g., by applying an appropriate voltage to the gate electrode, thus providing an opportunity to switch between destructive and constructive interference.

An alternative device structure might be to use an AlGaAs/GaAs heterostructure, at

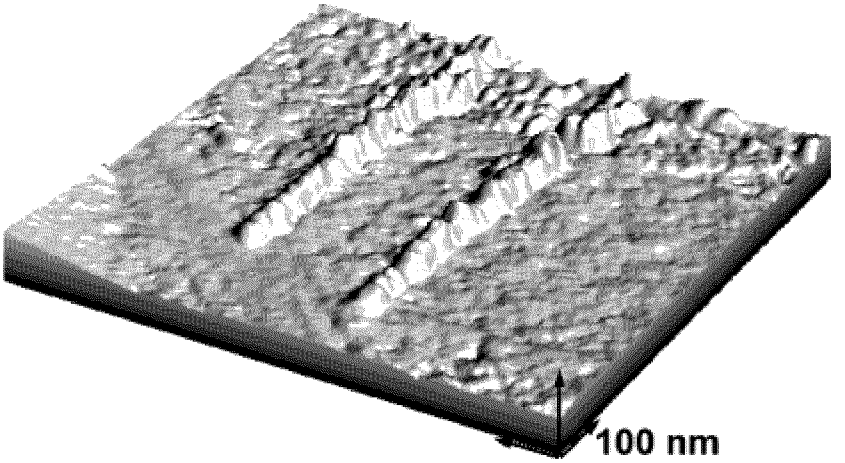

Fig 2. Two tungsten lines written onto a Si(111):H surface with the help of the field–induced decomposition of $W(CO)_6$ under the tip of a STM. The lines show a width of 20 nm and are some 800 nm in length.

which the AlGaAs capping layer is as thin as 30 – 40 nm in order to have the buried two–dimensional electron gas as close as possible to the surface. With the help of electrodes deposited on top and connected to a voltage source, the electron gas can be pre–confined to form a one–dimensional wire. If the AlGaAs material can locally be decomposed or even evaporated, this will result in the formation of a potential barrier in the one–dimensional electron channel. Being smaller than the width of this channel, the electrons are allowed to wend their way around this potential barrier, possibly also resulting in the development of interference phenomena. Indeed, it has recently been demonstrated that by using a laser grating method, structures of 300 nm can be fabricated owing to a laser–induced local decomposition of III–V semiconductors [5]. Detailed analyses show that the photon energy is mainly deposited in near–surface regions. Preliminary experiments using a STM revealed that by applying single-voltage pulses, 100–nm–wide pits can be formed in GaAs. Upon optimizing this process, the size of these features may significantly be reduced, thus making the 10–nm–range accessible.

3 Concluding remarks

Of course, it is usually a tough route to demonstrate the functionality of laboratory–built devices, but, hopefully, nanoparticles in conjunction with the unique capabilities of SPM provide a promising potential to pave the way for fabricating devices in terms of a bottom–up technology. Notwithstanding the feasibility of SPM in forming nanometer–scale structures, it should be kept in mind that the coherence length of electrons at room temperature is extremely small and typically falls below 10 nm, so that the operation of devices whose function is based on coherent transport is supposed to be limited to the very low–temperature regime.

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